Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.021”**

**.018”**

**51**

**G**

**D**

**S**

**Chip Back is also GATE**

**DRAIN and SOURCE are interchangeable**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0038” X .0038”**

**Backside Potential: GATE**

**Process 51**

**APPROVED BY: DK DIE SIZE .018” X .021” DATE: 10/20/21**

**MFG: FAIRCHILD THICKNESS .008” P/N: 2N4393**

**DG 10.1.2**

#### Rev B, 7/19/02